

# Design and Verification of AXI OCP Bridge Supporting Out-of-Order Transactions for achieving Dead Lock Free Communication

Author(s) Name: Shrikant, Roopa K.  
Bangalore, Karnataka

**Abstract**—Modern on-chip communication protocols such as advanced eXtensible Interface and open core protocol support advanced transactions to improve communication efficiency. Out-of-order transactions that allow responses to be returned in an order different from their request order play an important role in this improvement. However, a deadlock situation may occur if these transactions are not properly manipulated. In this paper, we address the deadlock problem in an on-chip bus system supporting out-of-order transactions. We present a graphic model that can well represent the status of a bus system and show that a cycle exists in the graph if and only if the bus system is in an unsafe state that may lead to a bus deadlock. Based on this model, we propose a novel bus design technique that can efficiently resolve the bus deadlock problem. Experimental result show that buses with the proposed technique can be up to 3.3 times faster than those with the currently available techniques.

**Index Terms**—Advanced eXtensible Interface (AXI), bus deadlock, on-chip bus, open core protocol (OCP), out-of-order execution, tagged transactions.

## I. INTRODUCTION

In the past decade, the advanced high-performance bus and advanced peripheral bus of advanced microcontroller bus architecture [1] are the most popular communication architectures for SOC designs. Both architectures are shared-link buses allowing only one master IP to access one slave IP at a time. Recently, the communication efficiency of shared link buses becomes insufficient because of their lack of parallel access capability. Some more advanced communication protocols such as advanced eXtensible Interface (AXI) [1] and open core protocol (OCP) [2] that facilitate parallel communication are thus proposed. Both AXI and OCP define communication interface protocols and transaction types but leave communication architecture to interconnect designers. Interconnect designers thus have the freedom to implement the communication protocols using multilayer, crossbar, networks-on-chip [3], or a combination of these designs to increase the communication parallelism. The communication protocols defined in AXI and OCP support various advanced transactions, including burst transactions, pipelined (outstanding) transactions, and out-of-order transactions [1], [2]. Among these transactions, the out-of-order transactions serve as a major key to improve system performance. Out-of-order transactions can be executed more efficiently when a master IP, such as a processor, can handle out-of-order returns as it allows a slave core such as a dynamic random-access memory controller to service requests in the order that is most convenient, rather than the order in which requests are sent by the master [2]. In [4] and [5], the authors show that by employing out-of-order mechanisms in memory controllers, the average execution time can be reduced by 21% to 41% over the conventional in-order memory accessing. Bus deadlock is a problem that

occurs when a set of IP cores communicating through a bus system are involved in a circular wait-and-hold state that cannot be resolved. This problem may crash a bus system as none of the IP cores involved in the deadlock can continue its functions. In [6], the authors invest the bus deadlock problem of a system that allows a master to execute a process only if the master is granted to access all required slaves of the process and each master will hold the slaves granted to it until all its required slaves are granted to it. A bus deadlock happens when each master in a set of masters is holding a slave and waiting for another slave held by another master in the set. In this type of bus deadlocks, the relation between masters and slaves is similar to that between processes and resources in an operating system (OS) where a deadlock occurs when there is a circular wait-and-hold relation among a set of processes and resources [7]. A resource allocation graph (RAG) is commonly utilized to represent the status of resource allocation in an OS [7]. A vertex in a RAG represents a process or a resource. A directed edge from a process vertex to a resource vertex denotes that the process is requesting the resource, and one from a resource vertex to a process vertex denotes that the resource is being held by the process. In an OS, a deadlock may occur when a cycle exists in the RAG [7]. In [6], the authors thus map the bus deadlock problem to the OS deadlock problem and propose a hardware approach which requires two to four clock cycles to detect the occurrence of a bus deadlock. In advanced bus/interface protocols such as AXI and OCP, a slave must return responses after some latency when it accepts a transaction request from a master. After the responses are returned and accepted, the transaction is completed and the slave must be released. As a result, a slave will be released from a master no matter whether the master is granted to access all its required slaves or not and thus the bus deadlock problem described in [6] does not happen in these protocols. However, another type of bus deadlock may occur because of the out-of-order transactions supported by these protocols. This is because in general a bus system supporting out-of-order transactions also needs to support transactions that do not allow out-of-order execution. For example, a read operation must wait for a preceding write operation if they address to the same memory location. Such read-after-write operations are commonly encountered in a bus system and they clearly do not allow out-of-order execution. To distinguish the transactions allowing and not allowing out-of-order, both AXI and OCP protocols define tagged transactions, in which a master tags an ID to each transaction in the way that the transactions whose responses must be returned in order are tagged with the same ID. A bus that fully supports the AXI or OCP protocol is responsible for assuring that the order of the responses returned to each master is the same as their request order if they have the same ID. Thus, the response returned by a slave may not be accepted by the bus and the slave has to wait until the order violation condition disappears. As a tagged transaction must wait for the completion of an earlier issued transaction with the same ID, it is possible that a set

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