

3.14 a. See Figure S.22.

Iteration	Instruction	Issues at	Executes/ Memory	Write CDB at	Comment
1	L.D F2,0(R1)	1	2	3	First issue
1	MUL.D F4,F2,F0	2	4	19	Wait for F2 Multi rs [3–4] Multi use [5–18]
1	L.D F6,0(R2)	3	4	5	Ldbuf [4]
1	ADD.D F6,F4,F6	4	20	30	Wait for F4 Add rs [5–20] Add use [21–29]
1	S.D F6,0(R2)	5	31		Wait for F6 Sbuf [16–31]
1	DADDIU R1,R1,#8	6	7	8	
1	DADDIU R2,R2,#8	7	8	9	
1	DSLTU R3,R1,R4	8	9	10	
1	BNEZ R3,foo	9	11		Wait for R3
2	L.D F2,0(R1)	10	12	13	Wait for BNEZ Ldbuf [11–12]
2	MUL.D F4,F2,F0	11	44 19	34	Wait for F2 Multi busy Multi rs [12–19] Multi use [20–33]
2	L.D F6,0(R2)	12	13	14	Ldbuf [13]
2	ADD.D F6,F4,F6	13	35	45	Wait for F4 Add rs [14–35] Add use [36–44]
2	S.D F6,0(R2)	14	46		Wait for F6 Sbuf [15–46]
2	DADDIU R1,R1,#8	15	16	17	
2	DADDIU R2,R2,#8	16	17	18	
2	DSLTU R3,R1,R4	17	18	20	
2	BNEZ R3,foo	18	20		Wait for R3
3	L.D F2,0(R1)	19	21	22	Wait for BNEZ Ldbuf [20–21]
3	MUL.D F4,F2,F0	20	23 34	49	Wait for F2 Multi busy Multi rs [21–34] Multi use [35–48]
3	L.D F6,0(R2)	21	22	23	Ldbuf [22]
3	ADD.D F6,F4,F6	22	50	60	Wait for F4 Add rs [23–49] Add use [51–59]

Figure S.22 Solution for exercise 3.14a.

Computer Architecture A Quantitative Approach Solution

John L. Hennessy, David A. Patterson



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