

Automatic Placement and Routing using Cadence Encounter

6.375 Tutorial 5
February 12, 2007

In this tutorial you will gain experience using Cadence Encounter to perform automatic placement and routing. A place+route tool takes a gate-level netlist as input and first determines how each gate should be placed on the chip. It uses several heuristic algorithms to group related gates together and thus hopefully minimize routing congestion and wire delay. Place+route tools will focus their effort on minimizing the delay through the critical path. To this end, these tools can resize gates, insert new buffers, and even perform local resynthesis. Place+route tools often have additional algorithms to help reduce area for non-critical paths. After placement, the place+route tool will attempt to route the design while minimizing wire delay. Place+route tools often include additional facilities for clock tree synthesis, power routing, and block level floorplanning. Figure 1 shows how Encounter fits into the 6.375 toolflow.

The following documentation is located in the course locker (`/mit/6.375/doc`) and provides additional information about Encounter and the Tower 0.18 μm Standard Cell Library.

- [tal-180nm-sc-databook.pdf](#) - Databook for Tower 0.18 μm Standard Cell Library
- [encounter-user-guide.pdf](#) - Encounter user guide
- [encounter-command-line-ref.pdf](#) - Encounter text command reference
- [encounter-menu-ref.pdf](#) - Encounter GUI reference

Getting started

Before using the 6.375 toolflow you must add the course locker and run the course setup script with the following two commands.

```
% add 6.375
% source /mit/6.375/setup.csh
```

For this tutorial we will be using an unpipelined SMIP^Sv1 processor as our example RTL design. You should create a working directory and checkout the SMIP^Sv1 example project from the course CVS repository using the following commands.

```
% mkdir tut5
% cd tut5
% cvs checkout examples/smipsv1-1stage-v
% cd examples/smipsv1-1stage-v
```

Before starting, take a look at the subdirectories in the `smipsv1-1stage-v` project directory. Figure 2 shows the system diagram which is implemented by the example code. When pushing designs through the physical toolflow we will often refer to the *core*. The core module contains everything which will be on-chip, while blocks outside the core are assume to be off-chip. For this tutorial we are assuming that the processor and a *combinational memory* are located within the core. A *combinational memory* means that the read address is specified at the beginning of the cycle, and

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Joacim Rocklöv



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VLSI-SoC: From Algorithms to Circuits and System-on-Chip Design Andreas Burg, Ayse Coskun, Matthew Guthaus, Srinivas Katkoori, Ricardo Reis, 2013-11-26 This book contains extended and revised versions of the best papers presented at the 20th IFIP WG 10.5 IEEE International Conference on Very Large Scale Integration VLSI SoC 2012 held in Santa Cruz CA USA in October 2012. The 12 papers included in the book were carefully reviewed and selected from the 33 full papers presented at the conference. The papers cover a wide range of topics in VLSI technology and advanced research. They address the current trend toward increasing chip integration and technology process advancements bringing about stimulating new challenges both at the physical and system design levels as well as in the test of these systems. **Energy-Efficient Communication Processors** Robert Fasthuber, Francky Catthoor, Praveen Raghavan, Frederik Naessens, 2013-05-29 This book describes a new design approach for energy efficient Domain Specific Instruction set Processor DSIP architectures for the wireless baseband domain. The innovative techniques presented enable co design of algorithms architectures and technology for efficient implementation of the most advanced technologies. To demonstrate the feasibility of the author's design approach case studies are included for crucial functionality of advanced wireless systems with increased computational performance flexibility and reusability. Designers using this approach will benefit from reduced development product costs and greater scalability to future process technology nodes. Euro-Par 2007 Workshops: Parallel Processing Luc Bougé, 2008-02-29 This book constitutes the thoroughly refereed joint post workshop proceedings of three international events: the International Workshop on Highly Parallel Processing on a Chip HPPC 2007, the UNICORE Summit 2007 and the Workshop on Virtualization Xen in High Performance Cluster and Grid Computing VHPC 2007 held in Rennes France in August 2007 within the scope of Euro Par 2007, the 13th International Conference on Parallel Computing. The 8 papers of the HHPC 2007 workshop address all aspects of existing and emerging envisaged multi core processors with a significant amount of parallelism especially to considerations on novel paradigms and models and the related architectural and linguistic support. The 8 papers presented at the UNICORE Summit 2007 show current developments and implementations of the UNICORE middleware system a grid technology providing a seamless secure and intuitive access to distributed Grid resources. UNICORE is a full grown and well tested Grid middleware system which today is used in daily production worldwide. The 9 papers of the VHPC 2007 workshop present new models for implementing high performance computing HPC architectures in both cluster and grid environments and cover areas including performance of virtual machine monitors VMM VMM architecture and implementation cluster and grid VMM applications management of VM based computing resources and hardware support for virtualization. Design Automation and Applications for Emerging Reconfigurable Nanotechnologies Shubham Rai, Akash Kumar, 2023-09-11 This book is a single source solution for anyone who is interested in exploring emerging reconfigurable nanotechnology at the circuit level. It lays down a solid foundation for circuits based on this

technology having considered both manual as well as automated design flows The authors discuss the entire design flow consisting of both logic and physical synthesis for reconfigurable nanotechnology based circuits The authors describe how transistor reconfigurable properties can be exploited at the logic level to have a more efficient circuit design flow as compared to conventional design flows suited for CMOS Further the book provides insights into hardware security features that can be intrinsically developed using the runtime reconfigurable features of this nanotechnology High Performance and Energy Efficient Multi-core Systems for DSP Applications Zhiyi Yu,2007 Data Acquisition Michele Vadursi,2010-11-28 The book is intended to be a collection of contributions providing a bird s eye view of some relevant multidisciplinary applications of data acquisition While assuming that the reader is familiar with the basics of sampling theory and analog to digital conversion the attention is focused on applied research and industrial applications of data acquisition Even in the few cases when theoretical issues are investigated the goal is making the theory comprehensible to a wide application oriented audience **FPGA ...** ,2006 EDN ,2005 **Dissertation Abstracts International** ,2007 Proceedings ,2004 *Automatic Datapath Tile Placement and Routing* Tatjana Serdar,2000

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