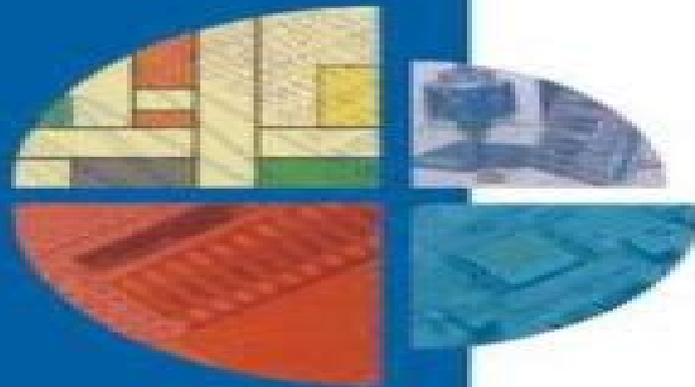


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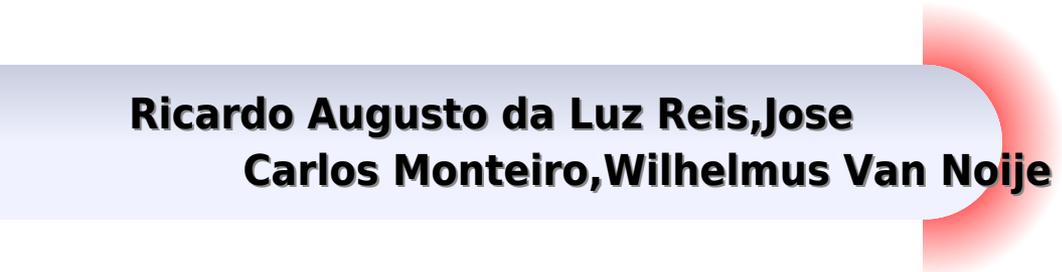


J. Vandenbussche  
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M. Steyaert

Springer-Science+Business Media, B.V.

# Systematic Design Of Analog Ip Blocks

**Ricardo Augusto da Luz Reis, Jose  
Carlos Monteiro, Wilhelmus Van Noije**



## **Systematic Design Of Analog Ip Blocks:**

**Systematic Design of Analog IP Blocks** Jan Vandenbussche, Georges Gielen, Michiel Steyaert, 2013-03-14 Systematic Design of Analog IP Blocks introduces a design methodology that can help to bridge the productivity gap Two different types of designs depending on the design challenge have been identified commodity IP and star IP Each category requires a different approach to boost design productivity Commodity IP blocks are well suited to be automated in an analog synthesis environment and provided as soft IP The design knowledge is usually common knowledge and reuse is high accounting for the setup time needed for the analog library Star IP still changes as technology evolves and the design cost can only be reduced by following a systematic design approach supported by point tools to relieve the designer from error prone repetitive tasks allowing him/her to focus on new ideas to push the limits of the design To validate the presented methodologies three different industrial strength applications have been selected and designed accordingly *Dynamic Characterisation of Analogue-to-Digital Converters* Dominique Dallet, José Machado da Silva, 2006-03-08 The Analogue to digital converter ADC is the most pervasive block in electronic systems With the advent of powerful digital signal processing and digital communication techniques ADCs are fast becoming critical components for system s performance and flexibility Knowing accurately all the parameters that characterise their dynamic behaviour is crucial on one hand to select the most adequate ADC architecture and characteristics for each end application and on the other hand to understand how they affect performance bottlenecks in the signal processing chain *Dynamic Characterisation of Analogue to Digital Converters* presents a state of the art overview of the methods and procedures employed for characterising ADCs dynamic performance behaviour using sinusoidal stimuli The three classical methods histogram sine wave fitting and spectral analysis are thoroughly described and new approaches are proposed to circumvent some of their limitations This is a must have compendium which can be used by both academics and test professionals to understand the fundamental mathematics underlining the algorithms of ADC testing and as an handbook to help the engineer in the most important and critical details for their implementation

*Matching Properties of Deep Sub-Micron MOS Transistors* Jeroen A. Croon, Willy M Sansen, Herman E. Maes, 2006-06-20 *Matching Properties of Deep Sub Micron MOS Transistors* examines this interesting phenomenon Microscopic fluctuations cause stochastic parameter fluctuations that affect the accuracy of the MOSFET For analog circuits this determines the trade off between speed power accuracy and yield Furthermore due to the down scaling of device dimensions transistor mismatch has an increasing impact on digital circuits The matching properties of MOSFETs are studied at several levels of abstraction A simple and physics based model is presented that accurately describes the mismatch in the drain current The model is illustrated by dimensioning the unit current cell of a current steering D A converter The most commonly used methods to extract the matching properties of a technology are bench marked with respect to model accuracy measurement accuracy and speed and physical contents of the extracted parameters The physical origins of microscopic fluctuations and how they

affect MOSFET operation are investigated This leads to a refinement of the generally applied 1 area law In addition the analysis of simple transistor models highlights the physical mechanisms that dominate the fluctuations in the drain current and transconductance The impact of process parameters on the matching properties is discussed The impact of gate line edge roughness is investigated which is considered to be one of the roadblocks to the further down scaling of the MOS transistor Matching Properties of Deep Sub Micron MOS Transistors is aimed at device physicists characterization engineers technology designers circuit designers or anybody else interested in the stochastic properties of the MOSFET

**Low-Power Deep Sub-Micron CMOS Logic** P. van der Meer,A. van Staveren,Arthur H.M. van Roermund,2012-12-06 1  
1 Power dissipation trends in CMOS circuits Shrinking device geometry growing chip area and increased data processing speed performance are technological trends in the integrated circuit industry to enlarge chip functionality Already in 1965 Gordon Moore predicted that the total number of devices on a chip would double every year until the 1970s and every 24 months in the 1980s This prediction is widely known as Moore s Law and eventually culminated in the Semiconductor Industry Association SIA technology road map 1 The SIA road map has been a guide for the in dustry leading them to continued wafer and die size growth increased transistor density and operating frequencies and defect density reduction To mention a few numbers the die size increased 7% per year the smallest feature sizes decreased 30% and the operating frequencies doubled every two years As a consequence of these trends both the number of transistors and the power dissipation per unit area increase In the near future the maximum power dissipation per unit area will be reached Down scaling of the supply voltage is not only the most effective way to reduce power dissipation in general it also is a necessary precondition to ensure device reliability by reducing electrical fields and device temperature to prevent device degradation A draw back of this solution is an increased signal propa gation delay which results in a lower data processing speed performance

**High-Speed Photodiodes in Standard CMOS Technology** Sasa Radovanovic,Anne-Johan Annema,Bram Nauta,2006-10-11 High speed Photodiodes in Standard CMOS Technology describes high speed photodiodes in standard CMOS technology which allow monolithic integration of optical receivers for short haul communication For short haul communication the cost aspect is important and therefore it is desirable that the optical receiver can be integrated in the same CMOS technology as the rest of the system If this is possible then ultimately a single chip system including optical inputs becomes feasible eliminating EMC and crosstalk problems while data rate can be extremely high The problem of photodiodes in standard CMOS technology it that they have very limited bandwidth allowing data rates up to only 50Mbit per second High speed Photodiodes in Standard CMOS Technology first analyzes the photodiode behaviour and compares existing solutions to enhance the speed After this the book introduces a new and robust electronic equalizer technique that makes data rates of 3Gb s possible without changing the manufacturing technology The application of this technique can be found in short haul fibre communication optical printed circuit boards but also photodiodes for laser disks *Wideband Low*

*Noise Amplifiers Exploiting Thermal Noise Cancellation* Federico Bruccoleri, Eric Klumperink, Bram Nauta, 2006-03-30 Low Noise Amplifiers LNAs are commonly used to amplify signals that are too weak for direct processing for example in radio or cable receivers Traditionally low noise amplifiers are implemented via tuned amplifiers exploiting inductors and capacitors in resonating LC circuits This can render very low noise but only in a relatively narrow frequency band close to resonance There is a clear trend to use more bandwidth for communication both via cables e.g. cable TV internet and wireless links e.g. satellite links and Ultra Wideband Band Hence wideband low noise amplifier techniques are very much needed Wideband Low Noise Amplifiers Exploiting Thermal Noise Cancellation explores techniques to realize wideband amplifiers capable of impedance matching and still achieving a low noise figure well below 3dB This can be achieved with a new noise cancelling technique as described in this book By using this technique the thermal noise of the input transistor of the LNA can be cancelled while the wanted signal is amplified The book gives a detailed analysis of this technique and presents several new amplifier circuits This book is directly relevant for IC designers and researchers working on integrated transceivers Although the focus is on CMOS circuits the techniques can just as well be applied to other IC technologies e.g. bipolar and GaAs and even in discrete component technologies

**Low-Power Low-Voltage Sigma-Delta Modulators in Nanometer CMOS** Libin Yao, Michiel Steyaert, Willy M. C. Sansen, 2006-02-06 this book is not suitable for the bookstore catalogue

**VLSI Circuits and Systems**, 2005

**The 5th IEE International Conference on ADDA 2005**, 2005 ADDA is a forum where experts in the field meet and exchange information on the developments in this field Due to recent growth in advanced Analogue to Digital and Digital to Analogue the topics covered were conversion techniques applications calibration testing standardisation and performance There is continuous improvement of higher speed and longer scale length devices together with new processing techniques to put more and more performance on the chip Together with this new techniques are being developed into new applications The driving force is the relentless move to replace analogue circuitry with digital

Book Review Index, 2004 Every 3rd issue is a quarterly cumulation

BMAS ..., 2004

**13th Symposium on Integrated Circuits and Systems Design** Ricardo Augusto da Luz Reis, Jose Carlos Monteiro, Wilhelmus Van Noije, 2000 These papers are taken from 13th Brazilian Symposium on Integrated Circuit Design SBCCI 2000 They address issues such as microarchitectures architecture logic design analogue design high level synthesis digital design physical modelling reconfigurable hardware and more

**Fourth International Symposium on Quality Electronic Design**, 2003 ISQED looks into the research development and application of design techniques and methods design processes and EDA design methodologies and tools that address issues that impact the quality of the realization of designs into physical integrated circuits It emphasizes a holistic approach toward design quality and to highlight and accelerate cooperation among the IC Design EDA Semiconductor Process Technology and Manufacturing communities

**The British National Bibliography** Arthur James Wells, 2003

**1995 URSI International Symposium on Signals, Systems, and Electronics**, 1995

Proceedings ,2003      *Electronic Design* ,2007      Books In Print 2004-2005 Ed Bowker Staff,Staff Bowker, Ed,2004  
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