

# Board Level Reliability of Chip Scale Packages

S.C. Hung, P.J. Zheng, H.N. Chen, S.C. Lee, and J.J. Lee  
Advanced Semiconductor Engineering, (ASE), Inc.  
26, Chin 3<sup>rd</sup> Rd., 811  
Nantze Export Processing Zone  
Kaohsiung, Taiwan  
Phone: 886-7-3617131 ext. 5210  
Fax: 886-7-3613094  
e-mail: Mike\_hung@asek.asetwn.com.tw

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## Abstract

*The joint fatigue life of PBGA, TFBGA, Film BGA, micro-BGA and BCC/BCC<sup>+</sup> is studied in this work. The effects of temperature profile, joint standoff, polyimide thickness, epoxy thickness, test board surface finish, and solder paste composition on the fatigue life are investigated. The temperature ramp rate has significant effect on the joint fatigue life. Attention should be paid not to reach the level of thermal shock. The effect of joint standoff can be predicted by shear strain energy density in the joint. The effect of polyimide thickness on the joint fatigue life is found to be more significant than does die paste thickness. The surface finish of test board also influences the fatigue life, although the difference between OSP and HASL is not significant. A 2% silver additive in the eutectic solder paste improves joint fatigue life. Different pad configurations induce different levels of stress concentration, and thus cause different levels of damage. This effect is found the same for both rigid- and flex-BGA. DNP effect is found to be very insignificant for both TF and Film BGA. However, the die edge effect is demonstrated to be tremendous. This can be due to the stress concentration and warpage near the edges of the chip caused by local CTE mismatch and the changes in flexural rigidity. Surface finish of test board affects the formation and the type of IMC. Different IMC affects joint fatigue life differently and cause different failure modes.*

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## Key words:

Chip Scale Package, Film BGA, TFBGA, Micro-BGA, BCC, Fatigue Life, and Reliability.

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## 1. Introduction

As portable electronic devices have become smaller, thinner, lighter, and more powerful in the recent years, the request of chip scale packages has become extremely high. However, since the packages have the characteristics of small and thin outline, and thus fine pitch and high density, the standoff of the solder interconnects becomes lower, the compliance of the solder joints degrades. Furthermore, the volume fraction of the chip in chip scale packages becomes larger, hence intensifies the thermal mismatch between the package and the motherboard. As a result, the fatigue life of the solder joint interconnection is under a

great impact due to the smaller pad size, lower standoff height, and greater thermal mismatch. Therefore, the second level reliability becomes a key issue for chip scale packages.

Recently, sizable efforts have been devoted to investigate the board level reliability of chip scale packages<sup>1-10</sup>. The fatigue life of a wide variety of CSP was reported<sup>1-5</sup>. The works cover a wide range of package types including rigid substrate CSP<sup>1-3</sup>, flex substrate CSP<sup>4-5</sup>, lead-frame CSP<sup>6</sup> and wafer level CSP<sup>6</sup>. The other attempt in predicting joint fatigue life is by evaluating the thermal stress induced in solder joint using numerical models<sup>7-10</sup>. Using Finite Element modeling, the package design can be optimized prior to package prototyping, however, the drawback is the verification and the validation of these models. Furthermore, process-related factors are difficult to be included into these models. Key factors affecting joint reliability were investigated and discussed extensively<sup>8-11,20</sup> for various Chip Scale packages. The factors investigated include die size<sup>8, 11,19,20</sup>, pad design<sup>8, 19,20</sup>, die paste<sup>8</sup>, solder shape<sup>8</sup>, solder composition<sup>8</sup>, underfill<sup>8, 11</sup>, board thickness<sup>8,19,20</sup>, and surface finish of test board<sup>19,21</sup>. As more chip scale packages are to be used in telecommunication products, the joint reliability under mechanical tests such as bend<sup>8, 21-22</sup> and drop<sup>23</sup> tests are gaining popularity. More recently, a work to discuss field and accelerated test conditions has been reported and

# Board Level Reliability Of Chip Scale Packages Imaps

**G Thomas**



## **Board Level Reliability Of Chip Scale Packages Imaps:**

Chiplet Design and Heterogeneous Integration Packaging John H. Lau,2023-03-27 The book focuses on the design materials process fabrication and reliability of chiplet design and heterogeneous integraton packaging Both principles and engineering practice have been addressed with more weight placed on engineering practice This is achieved by providing in depth study on a number of major topics such as chip partitioning chip splitting multiple system and heterogeneous integration with TSV interposers multiple system and heterogeneous integration with TSV less interposers chiplets lateral communication system in package fan out wafer panel level packaging and various Cu Cu hybrid bonding The book can benefit researchers engineers and graduate students in fields of electrical engineering mechanical engineering materials sciences and industry engineering etc

*Semiconductor Advanced Packaging* John H. Lau,2021-05-17 The book focuses on the design materials process fabrication and reliability of advanced semiconductor packaging components and systems Both principles and engineering practice have been addressed with more weight placed on engineering practice This is achieved by providing in depth study on a number of major topics such as system in package fan in wafer panel level chip scale packages fan out wafer panel level packaging 2D 2 1D 2 3D 2 5D and 3D IC integration chiplets packaging chip to wafer bonding wafer to wafer bonding hybrid bonding and dielectric materials for high speed and frequency The book can benefit researchers engineers and graduate students in fields of electrical engineering mechanical engineering materials sciences and industry engineering etc

*Area Array Interconnection Handbook* Karl J. Puttlitz,Paul A. Totta,2012-12-06 Microelectronic packaging has been recognized as an important enabler for the solid state revolution in electronics which we have witnessed in the last third of the twentieth century Packaging has provided the necessary external wiring and interconnection capability for transistors and integrated circuits while they have gone through their own spectacular revolution from discrete device to gigascale integration At IBM we are proud to have created the initial simple concept of flip chip with solder bump connections at a time when a better way was needed to boost the reliability and improve the manufacturability of semiconductors The basic design which was chosen for SLT Solid Logic Technology in the 1960s was easily extended to integrated circuits in the 70s and VLSI in the 80s and 90s Three I O bumps have grown to 3000 with even more anticipated for the future The package families have evolved from thick film SLT to thin film metallized ceramic to co fired multi layer ceramic A later family or ceramics with matching expansivity to sili con and copper internal wiring was developed as a predecessor of the chip interconnection revolution in copper multilevel submicron wiring Powerful server packages have been de veloped in which the combined chip and package copper wiring exceeds a kilometer All of this was achieved with the constant objective of minimizing circuit delays through short efficient interconnects

**The International Journal of Microcircuits and Electronic Packaging** ,2001 **Chip Scale Package (CSP)** John H. Lau,Shi-Wei Ricky Lee,1999 Featuring the latest design techniques plus details on more than 40 different types of CSP hands

engineers and designers the complete professional set of working tools to solve technical and design issues find the most efficient cost effective CSP solutions for deployments answer questions on interfacing speed robustness and more compare properties of wirebonds flip chips rigid and flex substrates wafer level redistribution and other CSP products get the latest information on new offerings from Fujitsu GE Hitachi IBM and other major companies and learn about CSP products under development

**Proceedings of the ... International Symposium on Microelectronics** ,2002 **International Symposium on Electronic Materials and Packaging** ,2000 Topics covered by this title include flip chip running solder joint reliability emerging technologies solder materials delimitation polymers for packaging design and process modelling and testing material characterization and package reliability

**Proceedings 2001** ,2001 *Journal of Microelectronics and Electronic Packaging* ,2004 **2000 International Symposium on Microelectronics** ,2000 This text constitutes proceedings from the International Symposium on Microelectronics that took place in Boston Massachusetts in September 2000

**Lead-free Solder Interconnect Reliability** Dongkai Shangguan,2005 This book provides the most up to date knowledge and data available on the reliability of lead free solder interconnects The content has been written by leading experts working in this important technology area Both fundamental research and practical considerations are addressed Environmental regulations are driving the worldwide adoption of lead free soldering technology for electronics packaging board assembly and related manufacturing operations While a significant amount of research and development work has been conducted in recent years on manufacturing issues to enable the conversion to lead free solders data from studies related to the reliability of lead free solder interconnects are still emerging Many research projects around the world have been undertaken to study lead free solder reliability under different loading conditions This book is the first comprehensive guide to reliability of lead free solder interconnects

2002 International Symposium on Microelectronics ,2002

*Packaging of Electronic and Photonic Devices* Gregory Joseph Kowalski,2000 *Reliability of RoHS-Compliant 2D and 3D IC Interconnects* John H. Lau,2010-10-22 Proven 2D and 3D IC lead free interconnect reliability techniques Reliability of RoHS Compliant 2D and 3D IC Interconnects offers tested solutions to reliability problems in lead free interconnects for PCB assembly conventional IC packaging 3D IC packaging and 3D IC integration This authoritative guide presents the latest cutting edge reliability methods and data for electronic manufacturing services EMS on second level interconnects packaging assembly on first level interconnects and 3D IC integration on microbumps and through silicon via TSV interposers Design reliable 2D and 3D IC interconnects in RoHS compliant projects using the detailed information in this practical resource Covers reliability of 2D and 3D IC lead free interconnects CCGA PBGA WLP PQFP flip chip lead free SAC solder joints Lead free SACX solder joints Low temperature lead free SnBiAg solder joints Solder joints with voids high strain rate and high ramp rate VCSEL and LED lead free interconnects 3D LED and 3D MEMS with TSVs Chip to wafer C2W bonding and lead free interconnects Wafer to wafer W2W bonding and lead free interconnects 3D IC chip stacking with low temperature

bonding TSV interposers and lead free interconnects Electromigration of lead free microbumps for 3D IC integration 3D IC Integration and Packaging John H. Lau,2015-07-06 A comprehensive guide to 3D IC integration and packaging technology 3D IC Integration and Packaging fully explains the latest microelectronics techniques for increasing chip density and maximizing performance while reducing power consumption Based on a course developed by its author this practical guide offers real world problem solving methods and teaches the trade offs inherent in making system level decisions Explore key enabling technologies such as TSV thin wafer strength measurement and handling micro solder bumping redistribution layers interposers wafer to wafer bonding chip to wafer bonding 3D IC and MEMS LED and complementary metal oxide semiconductor image sensors integration Assembly thermal management and reliability are covered in complete detail 3D IC Integration and Packaging covers 3D integration for semiconductor IC packaging Through silicon vias modeling and testing Stress sensors for thin wafer handling and strength measurement Package substrate technologies Microbump fabrication assembly and reliability 3D Si integration 2.5D 3D IC integration 3D IC integration with passive interposer Thermal management of 2.5D 3D IC integration Embedded 3D hybrid integration 3D LED and IC integration 3D MEMS and IC integration 3D CMOS image sensors and IC integration PoP chip to chip interconnects and embedded fan out WLP

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**The Journal of the Acoustical Society of America** Acoustical Society of America,2000 EDN ,1997 **Proceedings** ,1997 **Low Cost Flip Chip Technologies** John H. Lau,2000 Of the Standard NuBGA Packages Thinner

Substrate and Nonuniform Heat Spreader NuBGA Thermal Performance of the New NuBGA Package Temperature Distribution Thermal Resistance Cooling Power Wind Tunnel Experimental Analysis Solder Joint Reliability of the New NuBGA Package Electrical Performance of the New NuBGA Package Capacitance Inductance Summary of the New NuBGA Package Solder Bumped Flip Chip in PBGA Packages Intel's OLGA Package Technology OLGA Package Design OLGA Wafer Bumping OLGA Substrate Technology OLGA Package Assembly OLGA Package Reliability Mitsubishi's FC BGA Package

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