FPGA Implementation of Beamforming Receivers Based on MRC and NC-LMS for DS-CDMA System

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Abstract—In this paper, we investigate a beamforming receivers based on maximum ratio combining (MRC) and noise constraint least mean square (NC-LMS) using rapid prototyping method for FPGA implementation. Non-adaptive and adaptive beamforming techniques approaches are considered. A performance evaluation of these algorithms in a DS-CDMA system is presented and FPGA design is evaluated in term of hardware resources for Xilinx family devices using rapid prototyping methodology with Matlab-Simulink tools. Both approaches offer a good performance-complexity tradeoff favorable for FPGA implementation. However, due to the adaptive approach, the NC-LMS presents a better robustness to the fixed point arithmetic than the MRC.

1. Introduction

THE need, the quest for high-performance, high-speed, high-quality, high-reliability and most importantly low-cost systems drives the engineers to different and unlimited frontiers of battles of design and implementations. In this paper we face the problem of Beamforming or Smart Antennas (SA) design and implementation for DS-CDMA systems equipped with multiple receiving antennas.

SAs are recognized as a key technology for capacity increase in 3G radio networks. A SA's ability to abate both multipath and co-channel interference makes it one of the leading candidates [1] and one of the most promising technologies for the enabling of high capacity of the wireless networks, and interference cancellation. The most important contributions of an SA is its capability of changing its pattern in real time in order to track the user of interest with its maximum gain while trying to minimize the interference by placing the nulls of its radiation pattern at locations of the other users [2], i.e. the interferers.

Beamforming is the complex mathematical process standing behind that behavior of the antenna or the base station. We describe it as the backbone of the SA, or the main core of it. The beamforming is a process in which each user's signal is multiplied with appropriate weights that adjust the magnitude and the phase of the signal from each antenna. Hence the array forms a transmit beam in the desired direction and minimizes the output in other directions.

Considering the hardware implementation for beamforming algorithms, few past works have been reported. In [3], a reduced sampling rate beamforming technique for the reception of acoustic data transmitted through the water has been implemented on a DSP from Texas Instrument. In [4], the authors present an FPGA implementation using Xilinx devices and calibration methodologies for a smart antenna digital beamforming consisting of eight channels and operating in L band (1.6 to 2GHz). A comparison of efficient broadband beamforming architectures is presented in [5]; however no comparisons on hardware resource is reported. A low power ASIC implementation of 2Mbps antenna-rake combiner supporting both maximum ratio combining (MRC) and least mean square (LMS) filter is presented in [7] where a 107 MHz clock frequency and 550mW as highest rate power are achieved. In this paper, we implement both MRC and noise constrained LMS (NC-LMS) based beamforming techniques on FPGA, using rapid prototyping techniques (Matlab-Simulink). We evaluate the performance and hardware resource for both techniques.

This paper is organized as follows. A signal model is briefly described in Section 2. Beamforming techniques and performance evaluation using MRC and NC-LMS is presented in Section 3. The FPGA implementation and results of the beamforming techniques are described in Section 4. A conclusion is presented in Section 5.

2. Signal Model

Consider a reverse link from K mobile stations to a base station with multiple antennas. Let T represents the symbol interval; $s_{(k)}[n] \in S$ (S is the symbol alphabet; $S = \{\pm 1\}$ for binary phase shift keying (BPSK) case and $S = \{\pm 1/\sqrt{2} \pm j/\sqrt{2}\}$ for quadrature phase shift keying (QPSK) case) the nth symbol, and $d_{(k)}(\tau; n)$ the spreading waveform at the symbol of the kth transmission. The spreading waveform is written as

$$d_{(k)}(\tau; n) = \sum_{i=0}^{N-1} c_{(k)}[i; n] \varphi(\tau - iT_c) \quad \text{where} \quad T_c \text{ is the chip}$$

interval; $N = T/T_c$ the processing gain; $c_{(k)}[i; n]$ the ith element of the spreading sequence for the nth symbol of the kth transmission; and $\varphi(\tau)$ is the chip waveform of unit energy. Assume that the base station is equipped with L antenna elements and $\mathbf{a}(\theta)$ denotes the array response vector to the signal with angle of arrival (AOA) θ. The channel vector $\mathbf{h}_{(k)}$ can be written as $\mathbf{h} = \alpha \cdot \mathbf{a}(\theta)$. For Rayleigh fading channels α would be a complex Gaussian random variable. For M multipaths, there would be M spatial

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