

by Ray Marston

Field-Effect Transistors

Ray Marston looks at practical JFET circuits in this second episode of this four-part series.

Last month's opening episode explained (among other things) the basic operating principles of JFETs. JFETs are low-power devices with a very high input resistance and invariably operate in the depletion mode, i.e., they pass maximum current when the gate bias is zero, and the current is reduced ("depleted") by reverse-biasing the gate terminal.

Most JFETs are n-channel (rather than p-channel) devices. Two of the oldest and best known n-channel JFETs are the 2N3819 and the MPF102, which are usually housed in TO92 plastic packages with the connections shown in Figure 1; Figure 2 lists the basic characteristics of these two devices.

This month's article looks at basic usage information and applications of JFETs. All practical circuits shown here are specifically designed around the 2N3819, but will operate equally well when using the MPF102.

JFET BIASING

The JFET can be used as a linear amplifier by reverse-biasing its gate relative to its source terminal, thus driving it into the linear region. Three basic JFET biasing techniques are in common use. The simplest of these is the "self-biasing" system shown in Figure 3, in which the gate is grounded via R_g , and any current flowing in R_s drives the source positive relative to the gate, thus generating reverse bias.

Suppose that an I_D of 1mA is wanted, and that a V_{GS} bias of -2V is needed to set this condition; the correct bias can obviously be obtained by giving R_s a value of 2k Ω ; if I_D tends to fall for some reason, V_{GS} naturally falls as well, and thus makes it increase and counter the original change; the bias is thus self-regulating via negative feedback.

In practice, the V_{GS} value needed to set a given I_D varies widely between individual JFETs, and the only sure way of getting a precise I_D value in this system is to make R_s a variable resistor; the system is, however, accurate enough for many

applications, and is the most widely used of the three biasing methods.

A more accurate way of biasing the JFET is via the "offset" system of Figure 4(a), in which divider R_1 - R_2 applies a fixed positive bias to the gate via R_g , and the source voltage equals this voltage minus V_{GS} . If the gate voltage is large relative to V_{GS} , I_D is set mainly by R_s and is not greatly influenced by V_{GS} variations. This system thus enables I_D values to be set with good accuracy and without need for individual component selection.

Similar results can be obtained by grounding the gate and taking the bottom of R_s to a large negative voltage, as in Figure 4(b).

The third type of biasing system is shown in Figure 5, in which constant-current generator Q2 sets the I_D , irrespective of the JFET characteristics. This system gives excellent biasing stability, but at the expense of increased circuit complexity and cost.

In the three biasing systems described, R_g can have any value up to 10M Ω , the top limit being imposed by the volt drop across R_g caused by gate leakage currents, which may upset the gate bias.

SOURCE FOLLOWER CIRCUITS

When used as linear amplifiers, JFETs are usually used in either the source follower (common drain) or common-source modes. The source follower gives a very high input impedance and near-unity voltage gain (hence the alternative title of "voltage follower").

Figure 6 shows a simple self-biasing (via R_V1) source follower; R_V1 is used to set a quiescent R_2 volt-drop of 5V. The circuit's actual input-to-output voltage gain is 0.95. A degree of bootstrapping is applied to R_3 and increases its effective impedance; the circuit's actual input impedance is 10M Ω shunted by 10pF, i.e., it is 10M Ω at very low frequencies, falling to 1M Ω at about 16kHz and 100k Ω at 160kHz, etc.

Figure 7 shows a source follow-

Figure 1. Outline and connections of the 2N3819 and MPF102 JFETs.



Parameter	2N3819	MPF102
V_{DS} max (= max. drain-to-source voltage)	25V	25V
V_{DG} max (= max. drain-to-gate voltage)	25V	25V
V_{GS} max (= max. gate-to-source voltage)	-25V	-25V
I_{DS} (= drain-to-source current with $V_{GS} = 0V$)	2-20mA	2-20mA
I_{GS} max (= gate leakage current at 25 $^{\circ}$ C)	2nA	2nA
P_T max (= max. power dissipation, in free air)	200mW	310mW

Figure 2. Basic characteristics of the 2N3819 and MPF102 n-channel JFETs.

er with offset gate biasing. Overall voltage gain is about 0.95. C_2 is a bootstrapping capacitor and raises the input impedance to 48M Ω , shunted by 10pF.

Figure 8 shows a hybrid (JFET plus bipolar) source follower. Offset biasing is applied via R_1 - R_2 , and constant-current generator Q2 acts as a very high-impedance source load, giving the circuit an overall voltage gain of 0.99. C_2 bootstraps R_3 's effective impedance up to

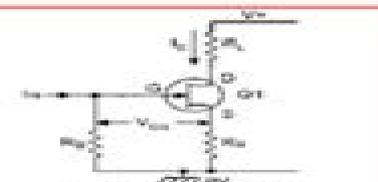


Figure 3. Basic JFET "self-biasing" system.

Figure 4. Basic JFET "offset-biasing" system.

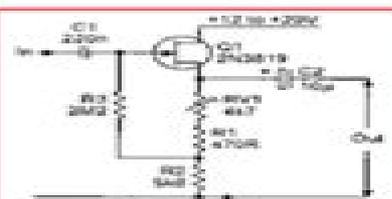


Figure 6. Self-biasing source-follower. $Z_{in} = 10M\Omega$.

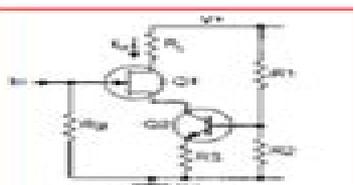


Figure 5. Basic JFET "constant-current" biasing system.

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Table of Contents Fet Principles And Circuits Ray Marston

1. Understanding the eBook Fet Principles And Circuits Ray Marston
 - The Rise of Digital Reading Fet Principles And Circuits Ray Marston
 - Advantages of eBooks Over Traditional Books
2. Identifying Fet Principles And Circuits Ray Marston
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Fet Principles And Circuits Ray Marston
 - User-Friendly Interface
4. Exploring eBook Recommendations from Fet Principles And Circuits Ray Marston
 - Personalized Recommendations
 - Fet Principles And Circuits Ray Marston User Reviews and Ratings
 - Fet Principles And Circuits Ray Marston and Bestseller Lists
5. Accessing Fet Principles And Circuits Ray Marston Free and Paid eBooks

- Fet Principles And Circuits Ray Marston Public Domain eBooks
 - Fet Principles And Circuits Ray Marston eBook Subscription Services
 - Fet Principles And Circuits Ray Marston Budget-Friendly Options
6. Navigating Fet Principles And Circuits Ray Marston eBook Formats
 - ePub, PDF, MOBI, and More
 - Fet Principles And Circuits Ray Marston Compatibility with Devices
 - Fet Principles And Circuits Ray Marston Enhanced eBook Features
 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Fet Principles And Circuits Ray Marston
 - Highlighting and Note-Taking Fet Principles And Circuits Ray Marston
 - Interactive Elements Fet Principles And Circuits Ray Marston
 8. Staying Engaged with Fet Principles And Circuits Ray Marston
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Fet Principles And Circuits Ray Marston
 9. Balancing eBooks and Physical Books Fet Principles And Circuits Ray Marston
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Fet Principles And Circuits Ray Marston
 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
 11. Cultivating a Reading Routine Fet Principles And Circuits Ray Marston
 - Setting Reading Goals Fet Principles And Circuits Ray Marston
 - Carving Out Dedicated Reading Time
 12. Sourcing Reliable Information of Fet Principles And Circuits Ray Marston
 - Fact-Checking eBook Content of Fet Principles And Circuits Ray Marston
 - Distinguishing Credible Sources
 13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development

- Exploring Educational eBooks
14. Embracing eBook Trends
- Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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