

FPGA and CPLD Architectures: A Tutorial

Recently, the development of new types of sophisticated field-programmable devices (FPDs) has dramatically changed the process of designing digital hardware. Unlike previous generations of hardware technology in which board level designs included large numbers of SSI (small-scale integration) chips containing basic gates, virtually every digital design produced today consists mostly of high-density devices. This is true not only of custom devices such as processors and memory but also of logic circuits such as state machine controllers, counters, registers, and decoders. When such circuits are destined for high-volume systems, designers integrate them into high-density gate arrays. However, the high non-recurring engineering costs and long manufacturing time of gate arrays make them unsuitable for prototyping or other low-volume scenarios. Therefore, most prototypes and many production designs now use FPDs. The most compelling advantages of FPDs are low startup cost, low financial risk, and, because the end user programs the device, quick manufacturing turnaround and easy design changes.

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This tutorial surveys some of the currently available, high-capacity, field-programmable devices. The authors describe the internal architectures of FPDs, simple and complex programmable logic devices, and field-programmable gate arrays. They then give architectural facts for the most important chips and describe applications of each type of device.

The FPD market has grown over the past decade to the point where there is now a wide assortment of devices to choose from. To choose a product, designers face the daunting task of researching the best uses of the various chips and learning the intricacies of vendor-specific software. Adding to the difficulty is the complexity of the more sophisticated devices. To help sort out the confusion, we provide an overview

of the various FPD architectures and discuss the most important commercial products, emphasizing devices with relatively high logic capacity.

Evolution of FPDs

The first user-programmable chip that could implement logic circuits was the programmable read-only memory (PROM), in which address lines serve as logic circuit inputs and data lines as outputs. Logic functions, however, rarely require more than a few product terms, and a PROM contains a full decoder for its address inputs. PROMs are thus inefficient for realizing logic circuits; so designers rarely use them for that purpose.

The first device developed specifically for implementing logic circuits was the field-programmable logic array, or simply PLA for short. A PLA consists of two levels of logic gates: a programmable, wired-AND plane followed by a programmable, wired-OR plane. A PLA's structure allows any of its inputs (or their complements) to be ANDed together in the AND plane; each AND plane output can thus correspond to any product term of the inputs. Similarly, users can configure each OR

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Table of Contents Computer Engineering Research Paper

1. Understanding the eBook Computer Engineering Research Paper
 - The Rise of Digital Reading Computer Engineering Research Paper
 - Advantages of eBooks Over Traditional Books
2. Identifying Computer Engineering Research Paper
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Computer Engineering Research Paper
 - User-Friendly Interface
4. Exploring eBook Recommendations from Computer Engineering Research Paper
 - Personalized Recommendations
 - Computer Engineering Research Paper User Reviews and Ratings
 - Computer Engineering Research Paper and Bestseller Lists

5. Accessing Computer Engineering Research Paper Free and Paid eBooks
 - Computer Engineering Research Paper Public Domain eBooks
 - Computer Engineering Research Paper eBook Subscription Services
 - Computer Engineering Research Paper Budget-Friendly Options
6. Navigating Computer Engineering Research Paper eBook Formats
 - ePub, PDF, MOBI, and More
 - Computer Engineering Research Paper Compatibility with Devices
 - Computer Engineering Research Paper Enhanced eBook Features
7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Computer Engineering Research Paper
 - Highlighting and Note-Taking Computer Engineering Research Paper
 - Interactive Elements Computer Engineering Research Paper
8. Staying Engaged with Computer Engineering Research Paper
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Computer Engineering Research Paper
9. Balancing eBooks and Physical Books Computer Engineering Research Paper
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Computer Engineering Research Paper
10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
11. Cultivating a Reading Routine Computer Engineering Research Paper
 - Setting Reading Goals Computer Engineering Research Paper
 - Carving Out Dedicated Reading Time
12. Sourcing Reliable Information of Computer Engineering Research Paper
 - Fact-Checking eBook Content of Computer Engineering Research Paper
 - Distinguishing Credible Sources
13. Promoting Lifelong Learning

- Utilizing eBooks for Skill Development
- Exploring Educational eBooks

14. Embracing eBook Trends

- Integration of Multimedia Elements
- Interactive and Gamified eBooks

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