PREVIOUS YEAR QUESTION PAPER
CS 405
COMPUTER SYSTEM ARCHITECTURE
MODULE 3 AND 4

DECEMBER 2018

1.a) Draw the state transition graph for a cache block using Goodman's write-once protocol for cache coherence.

 b) Design an 8 input omega network using 2X2 switches as building blocks. Show the switch settings for the permutation π1=(0,6,4,7,3)(1,5)(2). Show the conflicts in switch settings, if any. Explain blocking and non-blocking networks in this context.

2.a) Differentiate between synchronous and asynchronous model of linear pipeline processors.

 b) Consider the following pipeline reservation table:

	1	2	3	4
S1	X			X
S2		X		
S3			X	

i)   What are the forbidden latencies?
ii)   Draw the transition diagram.
iii)   List all the simple cycles and greedy cycles.
iv)   Determine the optimal constant latency cycle and minimal average latency (MAL)
v)   Let the pipeline clock period be τ=20ns. Determine the throughput of the pipeline.

3.a) Explain full-map directory based protocol.

b) What do you mean by dimension order routing? Consider a 16 node hypercube network. Based on E-cube routing algorithm, show how to route a message from 0010 to 1001. Find all intermediate nodes on routing path.

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