

Board Level Reliability of Chip Scale Packages

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Abstract

The joint fatigue life of PBGA, TFBGA, Film BGA, micro-BGA and BCC/BCC⁺ is studied in this work. The effects of temperature profile, joint standoff, polyimide thickness, epoxy thickness, test board surface finish, and solder paste composition on the fatigue life are investigated. The temperature ramp rate has significant effect on the joint fatigue life. Attention should be paid not to reach the level of thermal shock. The effect of joint standoff can be predicted by shear strain energy density in the joint. The effect of polyimide thickness on the joint fatigue life is found to be more significant than does die paste thickness. The surface finish of test board also influences the fatigue life, although the difference between OSP and HASL is not significant. A 2% silver additive in the eutectic solder paste improves joint fatigue life. Different pad configurations induce different levels of stress concentration, and thus cause different levels of damage. This effect is found the same for both rigid- and flex-BGA. DNP effect is found to be very insignificant for both TF and Film BGA. However, the die edge effect is demonstrated to be tremendous. This can be due to the stress concentration and warpage near the edges of the chip caused by local CTE mismatch and the changes in flexural rigidity. Surface finish of test board affects the formation and the type of IMC. Different IMC affects joint fatigue life differently and cause different failure modes.

Key words:

Chip Scale Package, Film BGA, TFBGA, Micro-BGA, BCC, Fatigue Life, and Reliability.

1. Introduction

As portable electronic devices have become smaller, thinner, lighter, and more powerful in the recent years, the request of chip scale packages has become extremely high. However, since the packages have the characteristics of small and thin outline, and thus fine pitch and high density, the standoff of the solder interconnects becomes lower, the compliance of the solder joints degrades. Furthermore, the volume fraction of the chip in chip scale packages becomes larger, hence intensifies the thermal mismatch between the package and the motherboard. As a result, the fatigue life of the solder joint interconnection is under a

great impact due to the smaller pad size, lower standoff height, and greater thermal mismatch. Therefore, the second level reliability becomes a key issue for chip scale packages.

Recently, sizable efforts have been devoted to investigate the board level reliability of chip scale packages¹⁻¹⁰. The fatigue life of a wide variety of CSP was reported¹⁻⁵. The works cover a wide range of package types including rigid substrate CSP¹⁻³, flex substrate CSP⁴⁻⁵, lead-frame CSP⁶ and wafer level CSP⁶. The other attempt in predicting joint fatigue life is by evaluating the thermal stress induced in solder joint using numerical models⁷⁻¹⁰. Using Finite Element modeling, the package design can be optimized prior to package prototyping, however, the drawback is the verification and the validation of these models. Furthermore, process-related factors are difficult to be included into these models. Key factors affecting joint reliability were investigated and discussed extensively^{8-11,20} for various Chip Scale packages. The factors investigated include die size^{8, 11,19,20}, pad design^{8, 19,20}, die paste⁸, solder shape⁸, solder composition⁸, underfill^{8, 11}, board thickness^{8,19,20}, and surface finish of test board^{11,17}. As more chip scale packages are to be used in telecommunication products, the joint reliability under mechanical tests such as bend^{8,11,21} and drop¹¹ tests are gaining popularity. More recently, a work to discuss field and accelerated test conditions has been reported and

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Table of Contents Board Level Reliability Of Chip Scale Packages Imaps

1. Understanding the eBook Board Level Reliability Of Chip Scale Packages Imaps
 - The Rise of Digital Reading Board Level Reliability Of Chip Scale Packages Imaps
 - Advantages of eBooks Over Traditional Books
2. Identifying Board Level Reliability Of Chip Scale Packages Imaps
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Board Level Reliability Of Chip Scale Packages Imaps
 - User-Friendly Interface
4. Exploring eBook Recommendations from Board Level Reliability Of Chip Scale Packages Imaps

- Personalized Recommendations
 - Board Level Reliability Of Chip Scale Packages Imaps User Reviews and Ratings
 - Board Level Reliability Of Chip Scale Packages Imaps and Bestseller Lists
5. Accessing Board Level Reliability Of Chip Scale Packages Imaps Free and Paid eBooks
 - Board Level Reliability Of Chip Scale Packages Imaps Public Domain eBooks
 - Board Level Reliability Of Chip Scale Packages Imaps eBook Subscription Services
 - Board Level Reliability Of Chip Scale Packages Imaps Budget-Friendly Options
 6. Navigating Board Level Reliability Of Chip Scale Packages Imaps eBook Formats
 - ePub, PDF, MOBI, and More
 - Board Level Reliability Of Chip Scale Packages Imaps Compatibility with Devices
 - Board Level Reliability Of Chip Scale Packages Imaps Enhanced eBook Features
 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Board Level Reliability Of Chip Scale Packages Imaps
 - Highlighting and Note-Taking Board Level Reliability Of Chip Scale Packages Imaps
 - Interactive Elements Board Level Reliability Of Chip Scale Packages Imaps
 8. Staying Engaged with Board Level Reliability Of Chip Scale Packages Imaps
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Board Level Reliability Of Chip Scale Packages Imaps
 9. Balancing eBooks and Physical Books Board Level Reliability Of Chip Scale Packages Imaps
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Board Level Reliability Of Chip Scale Packages Imaps
 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
 11. Cultivating a Reading Routine Board Level Reliability Of Chip Scale Packages Imaps
 - Setting Reading Goals Board Level Reliability Of Chip Scale Packages Imaps
 - Carving Out Dedicated Reading Time
 12. Sourcing Reliable Information of Board Level Reliability Of Chip Scale Packages Imaps

- Fact-Checking eBook Content of Board Level Reliability Of Chip Scale Packages Imaps
 - Distinguishing Credible Sources
13. Promoting Lifelong Learning
- Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
14. Embracing eBook Trends
- Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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