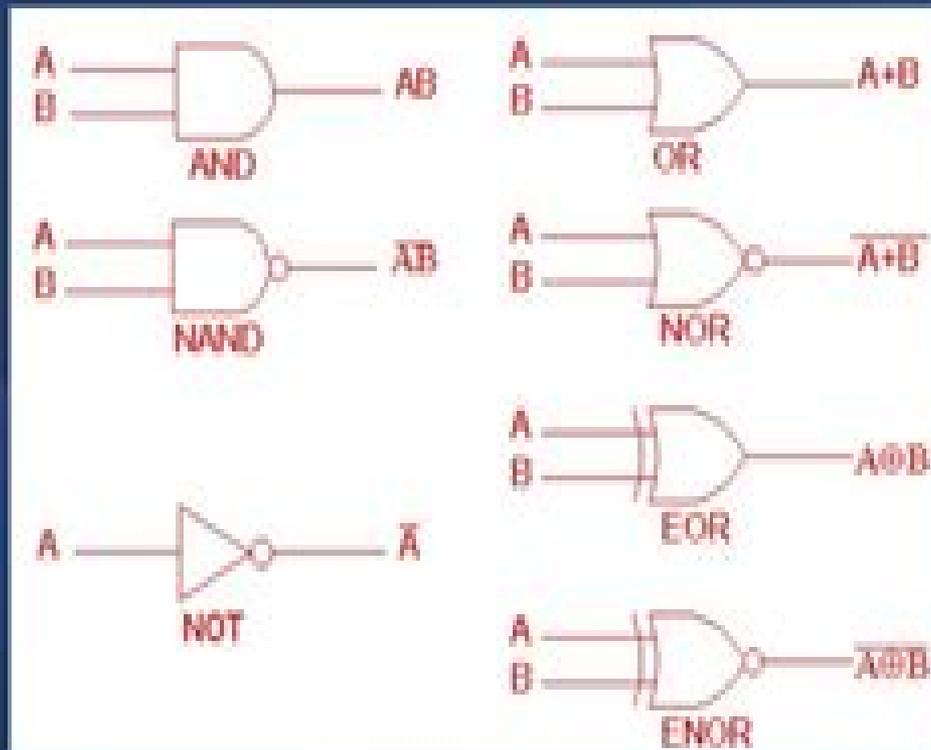


System Verilog Tutorial

Combinational Logic Design



```
// Code your design here
module test1m
input a, b, OR, AND, NAND, NOR, XOR, ENOR;
output logic y;
output reg OR, AND, NAND, NOR, XOR, ENOR;

always @(*)
begin
    assign OR = (a|b);
    $display("OR logical operator");

    assign AND = (a&b);
    $display("AND logical operator");

    assign XOR = (a^b);
    $display("XOR logical operator");

    assign NAND = ~(a&b);
    $display("NAND logical operator");

    assign NOR = ~(a|b);
    $display("NOR logical operator");

    assign XOR = ((a&b)^(a&~b));
    $display("XOR logical operator");

    assign ENOR = ~(a^b);
    $display("ENOR logical operator");
end
endmodule
```

Combinational Logic Design With Verilog

Mike Jess



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