PS

Zynq UltraScale+SoC

GIC (PL390)

Cortex-R5 32KB I/D L1 128KB TCM

RPU

Cortex-R5 32KB I/D L1 128KB TCM

GICv2

Cortex-A53 CPU Cluster

Core0 NEON — L1I$ L1D$
Core1 NEON — L1I$ L1D$
Core2 NEON — L1I$ L1D$
Core3 NEON — L1I$ L1D$

Timers

SCU

L2 Shared Cache

ACP

Configurable

Full Power Domain (FPD)

low Power Domain (LPD)

Security

Clocking

PS/PL Configuration

OCM Memory 265KB

Interconnect

USB 0/1
GigE 0/1/2/3
SDIO 0/1
UART 0/1
GPIO
CAN 0/1
I2C 0/1
SPI 0/1
QSPI 0/1
NAND ONFI 3.1
System Monitor

CMIO

EMIO

Interconnect

CCI Interconnect

Core Switch

Interconnect

GPU Mali-400

PCIe Gen2 x1/x2/x4

SATA0

SATA1

Display Port

2xS-AXI HPC

S-AXI ACE

S-AXI ACP-FPD

FPD_DMA

Interconnect

2xHPM FPD

4xS-AXI HP

HPM LPD

CSU DMA

SHA AES RSA

PMU

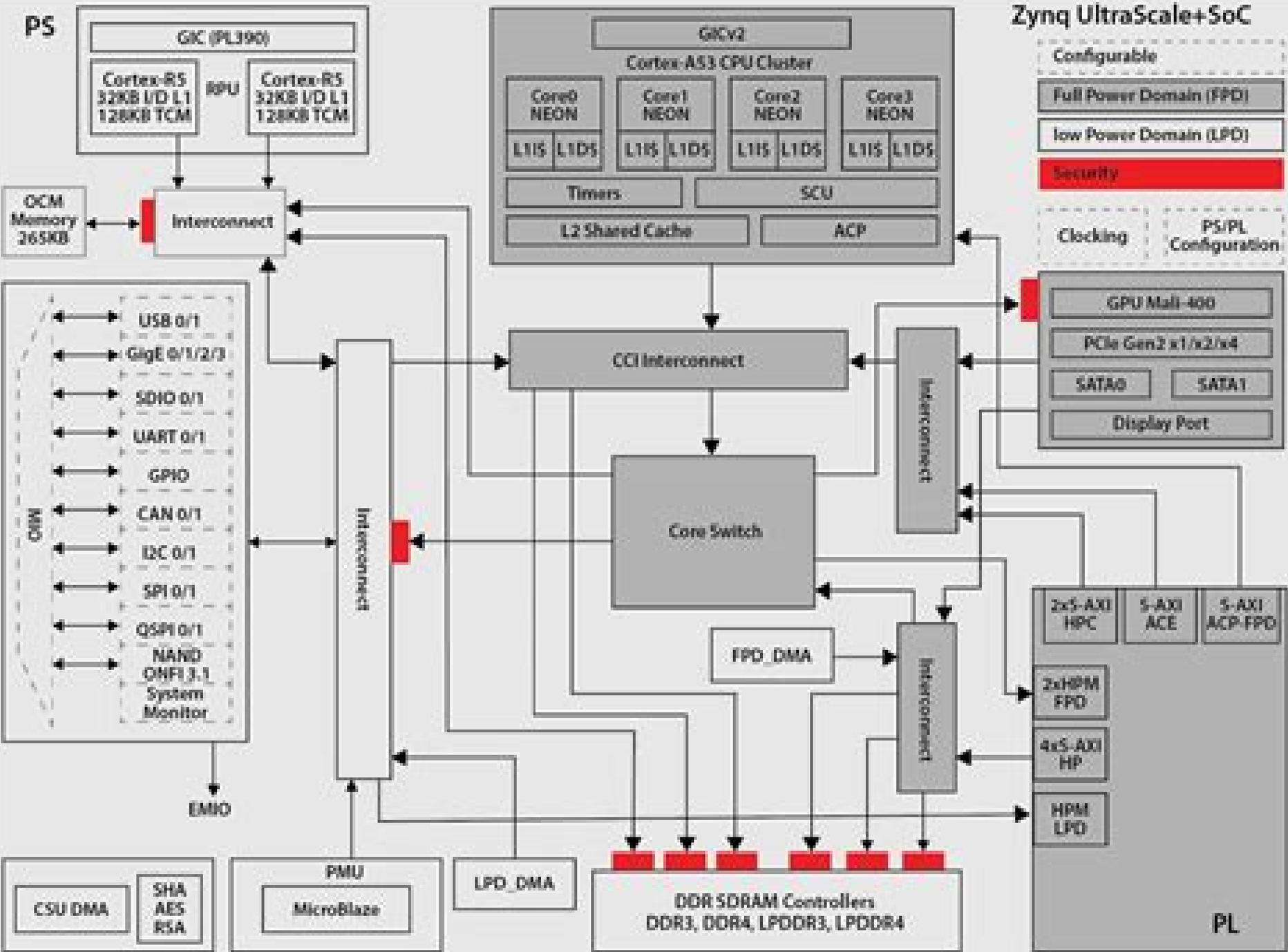MicroBlaze

LPD_DMA

DDR SDRAM Controllers
DDR3, DDR4, LPDDR3, LPDDR4

PL

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SB Merriam

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