



Crosstalk Aware Static Timing Analysis Environment

Joacim Rocklöv



Crosstalk Aware Static Timing Analysis Environment:

VLSI Design and Test Anirban Sengupta, Sudeb Dasgupta, Virendra Singh, Rohit Sharma, Santosh Kumar Vishvakarma, 2019-08-17 This book constitutes the refereed proceedings of the 23rd International Symposium on VLSI Design and Test VDAT 2019 held in Indore India in July 2019. The 63 full papers were carefully reviewed and selected from 199 submissions. The papers are organized in topical sections named analog and mixed signal design, computing architecture and security, hardware design and optimization, low power VLSI and memory design, device modelling and hardware implementation. **Microelectronics, Electromagnetics and Telecommunications** Jaume Anguera, Suresh Chandra Satapathy, Vikrant Bhateja, K.V.N. Sunitha, 2018-01-25 The volume contains 94 best selected research papers presented at the Third International Conference on Micro Electronics Electromagnetics and Telecommunications ICMEET 2017. The conference was held during 09-10 September 2017 at Department of Electronics and Communication Engineering BVRIT Hyderabad College of Engineering for Women Hyderabad Telangana India. The volume includes original and application based research papers on microelectronics, electromagnetics, telecommunications, wireless communications, signal speech video processing and embedded systems. **Test and Diagnosis for Small-Delay Defects** Mohammad Tehranipoor, Ke Peng, Krishnendu Chakrabarty, 2011-09-08 This book will introduce new techniques for detecting and diagnosing small delay defects in integrated circuits. Although this sort of timing defect is commonly found in integrated circuits manufactured with nanometer technology, this will be the first book to introduce effective and scalable methodologies for screening and diagnosing small delay defects including important parameters such as process variations, crosstalk and power supply noise.

High-Speed Interconnects in VLSI Design, Modeling, and Signal Integrity Dr. Bhaskar Gugulothu, The rapid advancement in VLSI Very Large Scale Integration technology has ushered in a new era of high performance systems where interconnects have become a critical bottleneck in determining speed, power and reliability. This textbook provides a comprehensive understanding of high speed interconnect design, analytical and simulation based modeling techniques and signal integrity challenges in modern integrated circuits. It is intended for graduate students, researchers and industry professionals involved in IC design and signal integrity analysis. **Dissertation Abstracts International**, 2002 **SSTA-SI** Bao Liu, 2007 We study signal integrity effects on statistical timing analysis e.g. interconnect and gate delay variations induced by crosstalk aggressor alignment i.e. difference in signal arrival times in coupled neighboring interconnects. Such effects bring significant source of variation and must be taken into account in statistical timing analysis. We establish a functional relationship between signal propagation delay and crosstalk alignment by deterministic circuit simulation and derive closed form formulas for statistical distributions of output signal arrival times. Our proposed method can be smoothly integrated into a static timing analyzer which runtime is dominated by sampling deterministic delay calculation while probabilistic computation and updating take constant time. Our experimental results on 70nm technology global interconnect structures

and 130nm technology industry designs show that lack of statistical crosstalk alignment consideration could lead to up to 114 65% 71 26% differences in interconnect delay means standard deviations and 159 4% 147 4% differences in gate delay means standard deviations while our method gives within 1 28% 3 38% mismatch in interconnect output signal arrival time means standard deviations and within 2 57% 3 86% mismatch in gate output signal arrival time means standard deviations respectively

An Iterative Crosstalk Aware Timing Analyzer Chih-Kuan Wang,2006 This thesis presents an iterative crosstalk aware timing analyzer Parameters such as slew rate voltage supply coupling capacitance and load capacitance are shown to affect gate delays in coupling structures The concept of relative signal arrival time and delay degradation curves is used to reduce pessimism in STA by Sasaki in 1 This thesis extends the work of Sasaki to an iterative algorithm while also considering dual supply voltges The algorithm uses empirical look up tables to model crosstalk noise The tables which include delays for three line structures are then mapped to any n line structure An initial solution is calculated in one pass Subsequent passes iteratively improve the solution by modeling delays outside the three line structure by changing the output loads of the outer lines in the three line structure This thesis proposes a iterative method of crosstalk aware timing analysis The results obtained by this method match HSpice simulation results very well

Proceedings of ASP-DAC/VLSI Design 2002 ,2002 Papers from a January 2002 conference are organized into four sessions each on low power design synthesis testing layout and interconnects and technology as well as two sessions each on embedded systems verification and VLSI architecture one session on analog design and one session on hot c

Static Crosstalk-Noise Analysis Pinhong Chen,Desmond A. Kirkpatrick,Kurt Keutzer,2013-11-20 As the feature size decreases in deep sub micron designs coupling capacitance becomes the dominant factor in total capacitance The resulting crosstalk noise may be responsible for signal integrity issues and significant timing variation Traditionally static timing analysis tools have ignored cross coupling effects between wires altogether Newer tools simply approximate the coupling capacitance by a 2X Miller factor in order to compute the worst case delay The latter approach not only reduces delay calculation accuracy but can also be shown to underestimate the delay in certain scenarios This book describes accurate but conservative methods for computing delay variation due to coupling Furthermore most of these methods are computationally efficient enough to be employed in a static timing analysis tool for complex integrated digital circuits To achieve accuracy a more accurate computation of the Miller factor is derived To achieve both computational efficiency and accuracy a variety of mechanisms for pruning the search space are detailed including Spatial pruning reducing aggressors to those in physical proximity Electrical pruning reducing aggressors by electrical strength Temporal pruning reducing aggressors using timing windows Functional pruning reducing aggressors by Boolean functional analysis

Proceedings of the ASP-DAC ... Asia and South Pacific Design Automation Conference ,2002

Design Signoff in the Era of 2nm: Architectures, Algorithms, and Automation 2025 Author1 : SRIKANTH AITHA, Author1 : DR. RAHUL KUMAR, PREFACE In the relentless pursuit of greater performance lower power

consumption and more compact form factors the semiconductor industry has once again reached a pivotal inflection point As process nodes push into the 2 nanometer realm the challenges of physical design signoffensuring that your layout not only functions correctly but also meets timing power and reliability requirements at manufacturable scale grow ever more formidable Variability at this scale is no longer a corner case it is the rule Interconnect resistance and capacitance dominate delay budgets Thermal and electromigration effects can emerge in unexpected hotspots And traditional signoff methodologies rooted in conservative margins and offline signoff engines strain under the weight of skyrocketing design complexity Design Signoff in the Era of 2 nm Architectures Algorithms and Automation is born of a simple conviction to navigate these challenges we must reinvent every facet of the signoff flow from the way we architect our design rule checks and timing models to the algorithms that solve them to the automation frameworks that orchestrate and accelerate the entire process This book is not a narrow recipe for using any single tool rather it is a comprehensive roadmap that unifies emerging best practices cutting edge research and real world case studies into a coherent vision of next generation signoff In these pages you will find Architectural Foundations A deep dive into the physical phenomena that dominate at 2 nm quantum confinement in channel materials interconnect parasitic and multi patterning variability and how they reshape the constraints of place and route and signoff engines

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Timing Analysis Yu Cao, 2000 *American Doctoral Dissertations*, 2000 **Frequency-aware Static Timing Analysis**

for Power-aware Embedded Architectures Kiran Ravi Seth, 2003 Keywords real time scheduling frequency scaling real time systems dynamic voltage scaling *Static Timing Analysis for Nanometer Designs* J. Bhasker, Rakesh

Chadha, 2009-04-03 iming timing timing That is the main concern of a digital designer charged with designing a semiconductor chip What is it how is it T described and how does one verify it The design team of a large digital design may spend months architecting and iterating the design to achieve the required timing target Besides functional verification the timing closure is the major milestone which dictates when a chip can be leased to the semiconductor foundry for fabrication This book addresses the timing verification using static timing analysis for nanometer designs The book has originated from many years of our working in the area of timing verification for complex nanometer designs We have come across many design engineers trying to learn the background and various aspects of static timing analysis Unfortunately there is no book currently available that can be used by a working engineer to get acquainted with the tails of static timing analysis The chip designers lack a central reference for information on timing that covers the basics to the advanced timing verification procedures and techniques

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