Cadence Tutorial D: Using Design Variables and Parametric Analysis

(Created for the NMSU VLSI program by Casey Wallace)
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Document Contents

Introduction

Design variables provide a method for specifying circuit parameters just before a simulation. This allows you to make quick changes to parameter values across single or multiple circuit components without having to edit any schematics schematic. Design variables can also be used to enable parametric analysis, which can sweep a design variable across a range of values and display multiple simulation results on a single plot.

Using Design Variables

This part of the tutorial will show you how to parameterize the width of the NMOS and PMOS transistors of an inverter by using design variables. These variable values are then set using the Analog Design Environment prior to simulation.

1. Make a copy of the inverter cell schematic you have previously designed, or create a new one.
2. Open the schematic of the inverter.
3. Left-click on the NMOS transistor to select it, and view its properties by center-clicking on it and selecting "Properties" (or you can press "q" as a shortcut).
4. Delete the text in the width box, and type wn. This specifies that a variable called wn will be used to set the width of the NMOS. When you do this, observe that values for "Drain/Source Diffusion Area" change from a constant value to a formula that involves the variable wn. Always check to make sure that formula is updated when you change the width to a variable, otherwise, your simulation results will be incorrect. Click **OK** to apply the change.
5. Repeat this procedure to change the width of the PMOS to wp.
6. Select Design → Check and Save. Verify that there are no errors.
7. Launch the Affirma Analog Design Environment.
8. Set up the simulation environment as you normally would for simulating a schematic. This includes specifying a stimulus file and transient run-length, enabling the SPICE netlist reader in the environment options, and selecting the outputs to be plotted on the schematic.
9. In ADE, select Variables → Copy From cellview. The design variables wn and wp should appear in the Design Variables area of the Analog Environment Window.
10. In ADE, select Variables → Edit. Left-click on wn in the value box, type $1.2u$ and then apply the value by clicking **Apply**. Change the value of wp to $2.4u$ and click **Apply**. Once the values have been assigned, click **OK**. See Figures 1 and 2 below.
11. In ADE, run the simulation by selecting Simulation → Netlist and Run. After waiting for the simulation to complete, the results window will pop up. The results should be

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