Compact modelling of noise for RF CMOS circuit design

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Abstract: The thermal noise of short-channel NMOS transistors in a commercially available 0.13-μm CMOS technology is studied. The experimental results are modelled with a non-quasi-static RF model, based on the principle of channel segmentation. The model is capable of predicting both drain and gate current noise accurately, without fitting any parameters to the measured noise data. An essential ingredient of the model is the gate resistance, which is shown to dominate the gate current noise. In the optimised device layouts, this gate resistance is mainly determined by the silicide-to-polysilicon contact resistance.

1 Introduction

The ever-continuing downscaling of CMOS technologies has resulted in a strong improvement in the RF performance of MOS devices [1–3]. Consequently, CMOS has become a viable option for analogue RF applications and RF system-on-chip. For the application of modern CMOS technologies in low-noise RF circuits, accurate modelling of noise is a prerequisite.

In MOSFETs, there are two intrinsic sources of noise: $1/f$ noise and thermal noise, the latter being the topic of this paper. Thermal noise is due to the random thermal motion of charge carriers. It not only manifests itself in the drain current noise spectrum, but, due to the capacitive coupling between channel and gate, also in the gate current noise spectrum. The latter effect is known as 'induced gate noise'. In addition to the intrinsic MOSFET thermal noise, the parasitic resistances (gate resistance, bulk resistance, and source/drain resistances) also exhibit thermal noise.

Thermal noise of deep-submicron MOSFETs has received considerable attention lately, triggered by publications reporting a strong enhancement of thermal noise with respect to long-channel theory [4–8]. In the earliest of these publications [4], thermal noise was found to be enhanced by a factor up to 12 in n-channel devices with gate length 0.7 μm, and hot electrons were proposed to explain these results. More recently, Klein [5, 6] reported very similar enhancement of drain current thermal noise in devices with gate length 0.65 μm and proposed a model that invokes heating of the charge carriers in the inversion channel to explain the experiments. For the induced gate noise, an even more dramatic enhancement factor as large as 30 was found by Knoblinger [7] for a 0.25-μm gate length n-channel MOSFET. Evidently, these reported noise enhancements would seriously limit the viability of RF CMOS, and a detailed study is called for.

In previous work [9–11], in sharp contrast to the above-mentioned authors, only moderate enhancement of the MOSFET drain current thermal noise was found, mainly caused by parasitic resistances and channel length modulation. This was found for 0.35-μm, 0.25-μm, and 0.18-μm CMOS technologies. MOSFET gate current thermal noise, on the other hand, was found to be enhanced more severely. This enhancement could be traced back to the effects of gate resistance, and the silicide-to-polysilicon contact resistance in particular.

Although the thermal noise, as found in CMOS fabrication down to 0.18 μm, seems fairly well understood, it remains important to study the phenomenon for more advanced CMOS technologies: it seems probable that at some point down the ITRS roadmap, the main assumption of our theory, i.e. thermal equilibrium, will break down. Therefore, in this work (which was reported earlier in [12]), we extend our study of MOSFET thermal noise to 0.13-μm technology. We present a large number of new experimental results in the 1–18 GHz frequency range, and compare them with the predictions of our previously developed RF MOSFET model.

2 Noise model

The model used in this paper has been described in detail in [11], therefore we will give only a short description here. The basis of the drain current thermal noise model is the well-known Klaassen–Prins equation [13], to which we have added the effects of channel length modulation, mobility reduction, and velocity saturation. The underlying assumptions are that (i) the charge carriers are in thermal equilibrium so that the voltage noise spectral density of a channel segment dx is given by the Nyquist expression $4k_\mathrm{B}T\mathrm{d}x/g(V)$, where $g(V)$ is the local channel conductance, and that (ii) the noise sources of different pieces of the channel are uncorrelated. Moreover, we neglect the possible noise contribution of the pinch-off region, in agreement with Jamal Deen et al. [14]. This is corroborated by the experimental observation that there is hardly any dependence of the noise on V_{DS} beyond the saturation voltage (see Section 3, Figs. 4c and 6c). All calculations were carried out in the framework of MOS model 11 [15, 16]. In the

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Compact Modelling in RF CMOS Technology Jun Liu,2011   **Cmos Rf Modeling, Characterization And Applications** M Jamal Deen,Tor A Fjeldly,2002-04-10 CMOS technology has now reached a state of evolution in terms of both frequency and noise where it is becoming a serious contender for radio frequency RF applications in the GHz range Cutoff frequencies of about 50 GHz have been reported for 0 18 m CMOS technology and are expected to reach about 100 GHz when the feature size shrinks to 100 nm within a few years This translates into CMOS circuit operating frequencies well into the GHz range which covers the frequency range of many of today s popular wireless products such as cell phones GPS Global Positioning System and Bluetooth Of course the great interest in RF CMOS comes from the obvious advantages of CMOS technology in terms of production cost high level integration and the ability to combine digital analog and RF circuits on the same chip This book discusses many of the challenges facing the CMOS RF circuit designer in terms of device modeling and characterization which are crucial issues in circuit simulation and design   *Device Modeling for Analog and RF CMOS Circuit Design* Trond Ytterdal,Yuhua Cheng,Tor A. Fjeldly,2003-08-01 Bridges the gap between device modelling and analog circuit design Includes dedicated software enabling actual circuit design Covers the three significant models BSIM3 Model 9 and EKV Presents practical guidance on device development and circuit implementation The authors offer a combination of extensive academic and industrial experience   **Small-signal Modeling of RF CMOS** Jaejune Jang,2004

Open Source TCAD/EDA for Compact Modeling Wladyslaw Grabinski,Daniel Tomaszewski,2018-04-13 The aim of this book is to highlight the benefits of a higher interoperability between Technology Computer Aided Design and Electronic Design Automation focusing on specifically selected open source tools for compact modeling Due to the tremendous developments in semiconductor technology in recent years device level modelling and integrated circuit design have become intimately related However they have been traditionally disconnected up to the circuit level This book consists of a set of extended user manuals guiding the reader from the usual software from multidimensional numerical process and device simulations through compact model development and its Verilog A standardization to carefully selected IC designs for analog radio frequency and digital applications Bringing together contributions from academic and industrial researchers and engineers the book forms a valuable reference for students and those working in the field   **FinFET/GAA Modeling for IC Simulation and Design** Yogesh Singh Chauhan,Chenming Hu,S. Salahuddin,Girish Pahwa,Avirup Dasgupta,Darsen Lu,Sriramkumar Vanugopalan,Ali Niknejad,Sourabh Khandelwal,Juan Pablo Duarte,Navid Payvadosi,2024-08-23 FinFET GAA Modeling for IC Simulation and Design Using the BSIM CMG Standard Second Edition is the first to book to explain FinFET modeling for IC simulation and the industry standard BSIM CMG describing the rush in demand for advancing the technology from planar to 3D architecture as now enabled by the approved industry standard The book gives a strong foundation on the physics and operation of FinFET details aspects of the BSIM CMG model such as surface potential charge

and current calculations and includes a dedicated chapter on parameter extraction procedures thus providing a step by step approach for the efficient extraction of model parameters With this book users will learn Why you should use FinFET The physics and operation of FinFET Details of the FinFET standard model BSIM CMG Parameter extraction in BSIM CMG FinFET circuit design and simulation and more Authored by the lead inventor and developer of FinFET and developers of the BSIM CMG standard model providing an expert s insight into the specifications of the standard A new edition of the original groundbreaking book on the industry standard FinFET model BSIM CMG New to This Edition Includes a new chapter providing a comprehensive introduction to GAAFET including motivations device concepts structure benefits and the industry standard GAAFET model Covers the most recent developments in the BSIM CMG model Presents an updated RF modeling of FinFET using the BSIM CMG model including parameter extraction Includes a new chapter on cryogenic modeling

Small-signal Modeling for CMOS Devices for RF Applications Ken Guo Yang,1999 **FinFET Modeling for IC Simulation and Design** Yogesh Singh Chauhan,Darsen Lu,Sriramkumar Vanugopalan,Sourabh Khandelwal,Juan Pablo Duarte,Navid Payvadosi,Ali Niknejad,Chenming Hu,2015-03-17 This book is the first to explain FinFET modeling for IC simulation and the industry standard BSIM CMG describing the rush in demand for advancing the technology from planar to 3D architecture as now enabled by the approved industry standard The book gives a strong foundation on the physics and operation of FinFET details aspects of the BSIM CMG model such as surface potential charge and current calculations and includes a dedicated chapter on parameter extraction procedures providing a step by step approach for the efficient extraction of model parameters With this book you will learn Why you should use FinFET The physics and operation of FinFET Details of the FinFET standard model BSIM CMG Parameter extraction in BSIM CMG FinFET circuit design and simulation Authored by the lead inventor and developer of FinFET and developers of the BSIM CM standard model providing an experts insight into the specifications of the standard The first book on the industry standard FinFET model BSIM CMG

Compact Modeling Gennady Gildenblat,2010-06-22 Most of the recent texts on compact modeling are limited to a particular class of semiconductor devices and do not provide comprehensive coverage of the field Having a single comprehensive reference for the compact models of most commonly used semiconductor devices both active and passive represents a significant advantage for the reader Indeed several kinds of semiconductor devices are routinely encountered in a single IC design or in a single modeling support group Compact Modeling includes mostly the material that after several years of IC design applications has been found both theoretically sound and practically significant Assigning the individual chapters to the groups responsible for the definitive work on the subject assures the highest possible degree of expertise on each of the covered models **MOSFET Modeling for Circuit Analysis and Design** Carlos Galup-Montoro,M rcio Cherem Schneider,2007 This is the first book dedicated to the next generation of MOSFET models Addressed to circuit designers with an in depth treatment that appeals to device specialists the book presents a fresh view of compact modeling

having completely abandoned the regional modeling approach Both an overview of the basic physics theory required to build compact MOSFET models and a unified treatment of inversion charge and surface potential models are provided The needs of digital analog and RF designers as regards the availability of simple equations for circuit designs are taken into account Compact expressions for hand analysis or for automatic synthesis valid in all operating regions are presented throughout the book All the main expressions for computer simulation used in the new generation compact models are derived Since designers in advanced technologies are increasingly concerned with fluctuations the modeling of fluctuations is strongly emphasized A unified approach for both space matching and time noise fluctuations is introduced   Small-signal Modeling for RF Si-CMOS Up to 40GHz I-Fan Wu,2004   **Modeling and Characterization of RF and Microwave Power FETs** Peter Aaen,Jaime A. Plá,John Wood,2007-06-25 This book is a comprehensive exposition of FET modeling and is a must have resource for seasoned professionals and new graduates in the RF and microwave power amplifier design and modeling community In it you will find descriptions of characterization and measurement techniques analysis methods and the simulator implementation model verification and validation procedures that are needed to produce a transistor model that can be used with confidence by the circuit designer Written by semiconductor industry professionals with many years device modeling experience in LDMOS and III V technologies this was the first book to address the modeling requirements specific to high power RF transistors A technology independent approach is described addressing thermal effects scaling issues nonlinear modeling and in package matching networks These are illustrated using the current market leading high power RF technology LDMOS as well as with III V power devices   Industry Standard FDSOI Compact Model BSIM-IMG for IC Design Chenming Hu,Sourabh Khandelwal,Yogesh Singh Chauhan,Thomas Mckay,Josef Watts,Juan Pablo Duarte,Pragya Kushwaha,Harshit Agarwal,2019-05-21 Industry Standard FDSOI Compact Model BSIM IMG for IC Design helps readers develop an understanding of a FDSOI device and its simulation model It covers the physics and operation of the FDSOI device explaining not only how FDSOI enables further scaling but also how it offers unique possibilities in circuits Following chapters cover the industry standard compact model BSIM IMG for FDSOI devices The book addresses core surface potential calculations and the plethora of real devices and potential effects Written by the original developers of the industrial standard model this book is an excellent reference for the new BSIM IMG compact model for emerging FDSOI technology The authors include chapters on step by step parameters extraction procedure for BSIM IMG model and rigorous industry grade tests that the BSIM IMG model has undergone There is also a chapter on analog and RF circuit design in FDSOI technology using the BSIM IMG model Provides a detailed discussion of the BSIM IMG model and the industry standard simulation model for FDSOI all presented by the developers of the model Explains the complex operation of the FDSOI device and its use of two independent control inputs Addresses the parameter extraction challenges for those using this model   **Low Power RF Circuit Design in Standard CMOS Technology** Unai Alvarado,Guillermo Bistué,Iñigo Adín,2011-10-18

Low Power Consumption is one of the critical issues in the performance of small battery powered handheld devices Mobile terminals feature an ever increasing number of wireless communication alternatives including GPS Bluetooth GSM 3G WiFi or DVB H Considering that the total power available for each terminal is limited by the relatively slow increase in battery performance expected in the near future the need for efficient circuits is now critical This book presents the basic techniques available to design low power RF CMOS analogue circuits It gives circuit designers a complete guide of alternatives to optimize power consumption and explains the application of these rules in the most common RF building blocks LNA mixers and PLLs It is set out using practical examples and offers a unique perspective as it targets designers working within the standard CMOS process and all the limitations inherent in these technologies   BSIM4 and MOSFET Modeling for IC Simulation Weidong Liu,Chenming Hu,2011 This book presents the art of advanced MOSFET modeling for integrated circuit simulation and design It provides the essential mathematical and physical analyses of all the electrical mechanical and thermal effects in MOS transistors relevant to the operation of integrated circuits Particular emphasis is placed on how the BSIM model evolved into the first ever industry standard SPICE MOSFET model for circuit simulation and CMOS technology development The discussion covers the theory and methodology of how a MOSFET model or semiconductor device models in general can be implemented to be robust and efficient turning device physics theory into a production worthy SPICE simulation model Special attention is paid to MOSFET characterization and model parameter extraction methodologies making the book particularly useful for those interested or already engaged in work in the areas of semiconductor devices compact modeling for SPICE simulation and integrated circuit design   Characterization and Modeling of a 0.13 Mikrometer CMOS Technology for RF Applications Wolfgang Berger,2005   **RF Modeling of Passive Components of an Advanced Submicron CMOS Technology** Nidhi Vashisht,2008   **Compact Models for Future Generation CMOS** Darsen Duane Lu,2011 Multiple gate MOSFETs with superior short channel control are expected to replace planar CMOS in the near future An accurate and computationally efficient compact transistor model is necessary to simulate circuits in multiple gate MOSFET technologies In this dissertation research a compact multiple gate MOSFET model BSIM MG is developed BSIM MG includes independent multi gate compact model BSIM IMG and common multi gate compact model BSIM CMG We focus on BSIM IMG for multiple gate MOSFETs with independent front and back gates The basic formulations for surface potential drain current and charge are derived and verified against TCAD simulations with excellent agreements The model preserves important property of multi gate MOSFETs such as volume inversion Non ideal effects including short channel effects length dependent back gate coupling transport models leakage currents parasitic resistances and capacitances temperature effects and self heating are considered in the model The model expressions are carefully formulated so that the symmetry of the source and drain is preserved Rules for maintaining symmetry are discussed in this dissertation For the common multi gate transistor model BSIM CMG the basic expressions have been improved so that it is

compatible with a novel non quasi static effects modeling technique charge segmentation In addition a parasitic source drain resistance model is developed including three components the contact resistance the spreading resistance and the bias dependent extension resistance Both BSIM CMG and BSIM IMG models are verified against TCAD and measured data The use of the FinFET compact model to model manufacturing variation in a FinFET technology is further explored The model matches measured data well for both the nominal case and the statistical distribution for NMOS threshold voltage as well as the read static noise margin A non Gaussian threshold voltage distribution is observed for nFET devices and the compact model successfully captures the distribution We further outlined and demonstrated a Monte Carlo based procedure for designing FinFET SRAM cells using the extracted variation information Technology scaling has enabled numerous CMOS analog circuits for low cost radio frequency applications The modeling of MOSFET thermal noise becomes very important In the final part of this dissertation research a new thermal noise model is developed for the industry standard BSIM4 model that enhances the existing thermal noise formulation in BSIM4 The model is verified against a segmented channel MOSFET model as well as measured data It is implemented in Berkeley SPICE3 and is ready for industry use A method to port the model to BSIM MG for thermal noise modeling in multi gate MOSFETs is also presented **RF and Microwave Modeling and Measurement Techniques for Field Effect Transistors** Jianjun Gao,2010-06-30 The purpose of this book is to introduce engineers and students to modern RF and microwave semiconductor device modelling and measurement techniques used in RF and microwave integrated circuit computer aided design CAD

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Table of Contents Compact Modelling In Rf Cmos Technology Doras Dcu

1. Understanding the eBook Compact Modelling In Rf Cmos Technology Doras Dcu
   - The Rise of Digital Reading Compact Modelling In Rf Cmos Technology Doras Dcu
   - Advantages of eBooks Over Traditional Books
2. Identifying Compact Modelling In Rf Cmos Technology Doras Dcu
   - Exploring Different Genres
   - Considering Fiction vs. Non-Fiction
   - Determining Your Reading Goals
3. Choosing the Right eBook Platform
   - Popular eBook Platforms
   - Features to Look for in an Compact Modelling In Rf Cmos Technology Doras Dcu
   - User-Friendly Interface
4. Exploring eBook Recommendations from Compact Modelling In Rf Cmos Technology Doras Dcu
   - Personalized Recommendations
   - Compact Modelling In Rf Cmos Technology Doras Dcu User Reviews and Ratings

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top index fund investing for small business for experts 3558
how to start ai image generator for creators for experts 3376
ultimate affiliate marketing for small business for experts 4469
how to use credit score improvement usa for students 4491
how to capsule wardrobe online for beginners 4128

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