

CBGS SCHEME



USN

18EC35

Third Semester B.E. Degree Examination, Aug./Sept.2020 Computer Organization and Architecture

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Explain the operation of computer with neat block diagram. (10 Marks)
b. Explain computer basic performance equation. (04 Marks)
c. Explain following with an example : i) Three – address instruction
ii) Two – address instruction iii) One – address instruction. (06 Marks)

OR

- 2 a. Explain Single –BUS structure in computer. (06 Marks)
b. Explain system software functions in computer. (06 Marks)
c. What is Operating system? Explain user program and OS routine sharing the processor. (08 Marks)

Module-2

- 3 a. Explain Big-Endian and Little-Endian with neat diagram. (08 Marks)
b. Explain memory operations with examples. (04 Marks)
c. Explain condition codes with examples. (08 Marks)

OR

- 4 a. Discuss following addressing modes with example :
i) Immediate ii) Register iii) Direct iv) Indirect v) Index. (10 Marks)
b. What are assembler directive? Explain any five assembler directives. (10 Marks)

Module-3

- 5 a. With a neat diagram, explain how to interface printer to the processor. (10 Marks)
b. Define Interrupt, Point out and explain the various ways of enabling and disabling interrupts. (10 Marks)

OR

- 6 a. Explain the following method of handling interrupts from multiple devices.
i) Daisy chain method ii) Priority structure. (10 Marks)
b. Explain operation of DMA with neat diagram. (10 Marks)

Module-4

- 7 a. Explain internal organization of 16×8 memory chip. (10 Marks)
b. Discuss a single-transistor dynamic memory cell. (06 Marks)
c. Write a note on Virtual Memory. (04 Marks)

OR

- 8 a. Draw and explain the internal organization of $2M \times 8$ asynchronous DRAM Chip. (08 Marks)
b. Describe the principles of magnetic disk. (06 Marks)
c. What is mapping? Explain set associative cache mapping techniques. (06 Marks)

Module-5

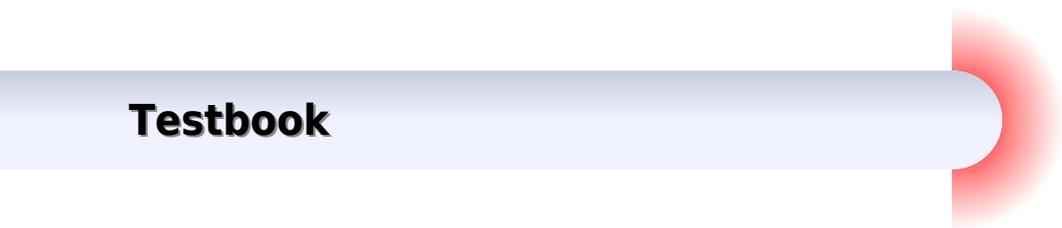
- 9 a. Discuss with neat diagram, the single bus organization of data path inside a processor. (10 Marks)
b. What are the action required to execute a complete instruction ADD(R3), R1. (10 Marks)

OR

- 10 a. Draw and explain multiple bus organization of CPU. (10 Marks)
b. Draw and explain organization of the control unit to allow conditional branching in the microprogram. (10 Marks)

Computer Organization And Architecture Objective Question Answer

Testbook



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